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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,508	10/03/2003	Yuen H. Chan	YOR920030142US1 (8728-623	1913

7590 10/04/2004

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EXAMINER	
AUDUONG, GENE NGHIA	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,508	CHAN ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Kuwazawa (U.S, Pat. No. 6,528,897).

Regarding claim 1, Kuwazawa discloses a static random access memory cell (Figure 1), comprising: a first and second passgate transistor (transistors 1 and 2); a first and second storage node (storage nodes between transistors 3, 5 and 4, 6), wherein the first passgate transistor 1 is connected between a first bit line 12 and a first storage node (node between transistors 3, 5), wherein a gate terminal of the first passgate transistor 1 connects to a word line 11, and the second passgate transistor 2 is connected between a second bit line 12 and the second storage node (node between transistors 4, 6), wherein a gate terminal of the second passgate transistor 2 connects to the word line 11; a first pull-up device (pull-up transistor 5), connected between a source voltage Vcc and the first storage node (storage node between transistors 3, 5); a second pull-up device (second pull-up transistor 6), connected between the source voltage Vcc and the second storage node (second storage node between transistors 4,6); first pull-down transistor (transistor 3), connected between the first storage node and a ground, wherein a gate terminal of the first pull-down transistor 3 is connected to the second storage node; and a second pull-down transistor (transistor 4), connected between the second storage node and the ground, wherein a

gate terminal of the second pull-down transistor 4 is connected to the first storage node; wherein the first and second passgate transistors (transfer transistors 1, 2) have first threshold voltages that are substantially the same, and wherein the first and second pull-down transistors (drive transistors 3, 4) have second threshold voltages that are substantially the same, and wherein the first threshold voltages are greater than the second threshold voltages (col. 3, lines 1+; col. 6, lines 4+).

Regarding claim 2 also claim 6, Kuwazawa discloses the memory cell having all of the limitation as of claim 1, wherein the first threshold voltages are about 0.7 V and the second threshold voltages are about 0.3 V (cited reference discloses the threshold voltages are ranging from 0.75v – 0.95v and 0.6v – 0.8v and varying to increase or decrease the voltage level based on the beta (β) factor that require for the circuit is met as claimed for the voltage range; col. 4, lines 10+; col. 1, lines 17+; col. 5, lines 48+).

Regarding claim 3, Kuwazawa discloses the memory cell having all of the limitation as of claim 1, wherein the first and second passgate transistor 1, 2 have first channel widths that are substantially the same and wherein the first and second pull-down transistor 3, 4 have second channel widths that are substantially the same, wherein the second channel widths are greater than the first channel widths (col. 1, lines 17-33).

Regarding claims 4-5, Kuwazawa discloses the memory cell having all of the limitation as of claim 1, wherein the first and second passgate transistor 1, 2 have first channel widths that are substantially the same (transfer transistors 1, 2 having gate width/gate length 0.18/0.18, therefore, their channel widths are substantially the same), and wherein the first and second pull-down transistor have second channel widths that are substantially the same (drive transistors 3, 4

having gate width/gate length 0.22/0.18, therefore, drive transistors' channel widths are substantially the same), wherein the memory cell has a cell beta ratio of about 3.0; or wherein the second channel widths and the first channel widths are substantially the same and a cell beta ration is about 1 (the beta ratio of memory cell to determining the stability or sensitivity of memory cell; the higher beta ratio the more stable and the lower the beta ratio the more sensitive. Therefore, the beta ratio for the cell is selected based on the requirement of the device, to have a sensitive memory cell or to have more stable cell).

Regarding claim 7, Kuwazawa discloses the memory cell having all of the limitation as of claim 6, wherein the memory cell size is about 2.40 Um2 (cell size in the device varying base on the beta ratio that requirement for the device).

Regarding claim 8, Kuwazawa discloses the memory cell having all of the limitation as of claim 1, wherein the first pull-up device (transistor 5) is a first pull-up transistor and second pull-up device (transistor 6) is a second pull-up transistor, and wherein a gate terminal of the first pull-up transistor 5 connects to the second storage node (node between transistors 4 and 6) and a gate terminal of the second pull-up transistor 6 connects to the first storage node (node between transistors 3 and 5).

Claims 9-15 and 16-22 contain the similar limitation as previously discussed in claims 1-8. Therefore, they are analyzed as previously discussed with respect to claims 1-8.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
September 22, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818